Jitters on HDMI to SDI Conversion

Although HDMI and SDI are both digital and seem to share similar eye pattern waveforms, they are completely different technologies except that they look alike! SDI is a much older technology which has been prevailing and dominating the broadcasting industries for decades. The underlying technique to transmit SDI signal is based on scrambler, serialization, de-scrambler, and of course de-serialization! Meantime, since SDI technology is more like fixed bit rate transmission mechanism, typically 270Mbps, 1.485Gbps, and now 2.97Gbps, there is actually a more stringent requirement on jitters for SDI signals! This requirement is especially vital for SDI, because in this realm, there is only one coaxial cable or one transmission path for both clock and data. State-of-the-art DisplayPort technology actually shares more of this fixed bit rate spirit than TMDS, which is the backbone of HDMI transmission technology! Silicon Image has made a significant contribution to develop TMDS, Transition Minimized Differential Signaling, and nowadays, this technique is widely adopted in typical interfaces such as DVI and HDMI! There is a huge and obvious difference for transmitting TMDS and SDI, which is the number of pairs of transmission path.

As mentioned above, SDI uses only up to one pair of lines, which normally requires only one coaxial cable whereas TMDS uses 4 pairs of lines, 3 for data and 1 for reference clock! It is readily easy to realize that those techniques present very different underlying complexities and therefore different requirements on signal integrity.

Typically, the clock of TMDS consumes only 1⁄10 of the bandwidth of the rest of data lines. Apparently, this lower requirement on bandwidth is very helpful to simplify the clock recovery circuits and loosen the requirement on clock jitters. This framework actually works very well for normal TMDS transmission. However, for HDMI to SDI conversion, the situation becomes difficult for SDI signaling. On the next page, 2 tables are for jitter requirements for both techniques. To make things easier to understand, we can treat UI and Tbit as the same unit to measure jitters. We can think of the units as percentage! For instance, 0.2 UI means 20% variation and 0.15 Tbit for 15%. Apparently, those numbers look close, but unfortunately, they do not share the same physical meaning! As explained in the above sentences, the clock speed is only 1⁄10 of that of data in TMDS transmission! However, for SDI, clock and data share the same transmission media, and the clock actually runs the same speed as data! This is critical and means even for the same bit rate, SDI actually places around 10 time stringent requirement on clock jitters than TMDS does! Considering that HDMI spec does not specify data jitter numerically, this will make things more

unpredictable after transformation. The situation gets worse for 3G SDI!

TMDS

Table 4-16 Source AC Characteristics at TP1

Item	Value
Rise time / fall time (20%-80%)	75psec ≤ Rise time / fall time ≤ 0.4 T_{bit}
Undershoot, max	25% of full differential amplitude (V_{swing}*2)
Intra-Pair Skew at Source Connector, max	0.15 T_{bit}
Inter-Pair Skew at Source Connector, max	0.20 $T_{character}$
Clock duty cycle, min / average / max	40% / 50% / 60%
TMDS Differential Clock Jitter, max	0.25 T_{bit} (relative to Ideal Recovery Clock as defined in Section 4.2.3)

The design of a Source should take into account the differential impedance of the cable assembly and Sink of 100 ohms (see Table 4-21).

SDI

Table 5 – Jitter specifications

B1	10 Hz	Timing jitter lower band edge	
B2	100 kHz	Alignment jitter lower band edge	
B3	> 1/10 the clock rate	Upper band edge	
A1	1 UI	Timing jitter	(Note 1)
A2	.2 UI	Alignment jitter (UI = unit interval)	
Test signal	Color bar test signal		(Note 2)
n	≠ 10 (preferred)	Serial clock divided	(Note 3)

NOTES

1 Designers are cautioned that parallel signals conforming to interconnection standards, such as SMPTE 260M, may contain jitter up to 2 ns p-p. Direct conversion of such signals from parallel to serial could result in excessive serial signal jitter.

2 Color bars are chosen as a nonstressing test signal for jitter measurements. Use of a stressing signal with long runs of zeros may give misleading results.

3 Use of a serial clock divider value of 10 may mask word correlated jitter components.

4 See SMPTE RP 184 for definition of terms.

If we consider more that there are 3 pairs of lines to transmit TMDS and only one for SDI, the TMDS data bit rate can run only at 1⁄3 of speed of that of SDI. Of course, those factors can be considered when designing the HDMI to SDI converters! However, for the reality, there are millions of HDMI sources either complaint or not with HDMI spec, asking HDMI to SDI converters to work with all HDMI players and SDI displays under these physical limitations resulting from typical commodity video players, such as Blue-ray player or DVD player and professional SDI monitors, is basically very hard to be practical. Especially, the cost is always the first factor to be brought up for consumer electronics, jitters might be something designers could ignore subconsciously under **cost** and **short range transmission** consideration when designing HDMI sources.

Despite of different units for measurement of jitters and types of jitters in terms of different bandwidths, the profound effects coming from physical layer make the HDMI to SDI conversion is difficult to fulfill the SDI jitter requirement and therefore hard to guarantee the stability after transformation. If the eye patterns are not as good as expected, what will happen to SDI transmission? Nobody knows. Perhaps, a good receiver with built-in equalizer and re-timer may handle it! However, even a well designed re-timing circuit has its limitation. For high speed signals such as 3G, 0.4 UI or 0.5UI are too much for a clock recovery circuit for current technologies at a reasonable and affordable price! Therefore, for such a product category, to use HDMI sources with reasonably lower jitters is very crucial to get systems to be built up!